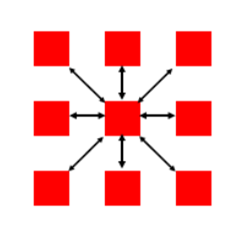
**EENG 5560**

**ASSIGNMENT 3**

**Assigned – February 16, 2023**

**Due – February 23, 2023**

Each red block shown in the figure below represents a computational unit (CU). Each CU can perform Addition, Subtraction, Multiplication, Greater Than, Less Than and Equal to operations. Each CU can exchange data with its immediate neighbors (top, bottom, left, right and diagonally).



* Use Xilinx Vivado to design and simulate the logic shown above.
* Inputs are 4-bit wide.
* Make sure you test your design for all the operations listed above.

Submit vhdl code, RTL schematic, screenshots of simulation waveforms, and test bench of the design. Test your design using at least five test cases. Mark two of the test cases and show the corresponding inputs, expected outputs and simulated outputs for those two cases. The source files should contain appropriate comments for better understanding.